DYNAMIC CMOS LEVEL-SHIFTING CIRCUIT APPARATUS

Abstract of the Disclosure

A dynamic CMOS level shifter circuit apparatus in a digital electronic system is disclosed for shifting a signal of a first logic family at a first lower voltage level to a second higher voltage level for a second logic family. The shifter circuit apparatus comprises a first transistor pair that has a first PMOS and a first NMOS transistor connected in series; a second transistor pair that has a second PMOS and a second NMOS transistor connected in series; and a power-down control PMOS transistor. The first and second transistor pairs are connected in parallel, and the parallel connection is connected in series with the power-down control PMOS transistor across the power and ground level of the system. The node at which the drain terminals of the transistors of the first transistor pair is connected together is also connected to the gate of the second PMOS transistor. The node at which the drain terminals of the transistors of the second transistor pair is connected together is also connected to the gate of the first PMOS transistor. Further, the gate terminal of the first NMOS transistor serves as the signal input for the input logic family, and the gate terminal of the first PMOS transistor serves as the shifted output of the shifter circuit apparatus.

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